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December 29, 2006
Date of Signature

Re:	Application of:	Jenoe Tihanyi
	Serial No.:	10/757,974
	Filed:	January 15, 2004
	For:	MOSFET Circuit Having Reduced Output Voltage Oscillations During a Switch-Off Operation
	Group Art Unit:	2816
	Examiner:	Hiep Nguyen
	Our Docket No.:	1890-0033

TRANSMITTAL OF BRIEF ON APPEAL

Please find for filing in connection with the above patent application the following documents:

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Respectfully Submitted,

MAGINOT, MOORE & BECK, LLP

December 29, 2006

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Enclosures

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BRIEF ON APPEAL

Sir:

This is an appeal under 37 CFR § 41.31 to the Board of Patent Appeals and Interferences of the United States Patent and Trademark Office from the rejection of claims 15 and 18-35 of the above-identified patent application. Claims 15 and 18-35 were finally rejected in the Office Action dated July 26, 2006. A check in the amount of **$500.00** is enclosed herewith to cover the fee required under 37 CFR § 41.20(b)(2). Also, please provide any extension of time which may be necessary and charge any fees which may be due to Deposit Account No. 13-0014, but not to include any payment of issue fees.

(1) REAL PARTY IN INTEREST

Infineon Technologies AG is the owner of this patent application, and therefore is the real parties in interest.

(2) RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences in this case.

(3) STATUS OF CLAIMS

Claims 15 and 18-35 are pending in the application.

Claims 15 and 18-35 stand rejected and form the subject matter of this appeal. Claims 15 and 18-35 are shown in the Appendix attached to this Appeal Brief.

(4) STATUS OF AMENDMENTS

A preliminary amendment was filed on January 15, 2004. A first Office Action was mailed February 17, 2005, which failed to consider the preliminary amendment. Applicants filed a Response to Office Action dated May 17, 2005 ("First Response") responsive to the Office Action dated February 17, 2005. A second Office Action dated July 29, 2005 was designated by the Examiner to be responsive to the First Response. Applicants filed a response to the July 29, 2005 office action on October 31, 2005 ("Second Response"). A third Office Action dated January 9, 2006 was designated by the Examiner to be responsive to the Second Response. Applicant filed a response to the January 9, 2006 office action on April 10, 2006 ("Third Response"). A final office action dated July 26, 2006 ("Final Office Action") was designated by the Examiner to be responsive to the Third Response.

(5) SUMMARY OF THE CLAIMED SUBJECT MATTER

Independent claim 15 is directed to a MOSFET circuit that includes first and second MOS transistors and a Zener diode. The first MOS transistor has a first number of cells, and the second MOS transistor has a second, lesser number of cells. By way of non-limiting example, Fig. 1 of the Application shows a MOSFET circuit having a first MOS transistor T1 and a second MOS transistor T2. (See Specification at p.4, line 21-23). The second transistor T2 has a lesser number of cells than the first transistor T1. (See *id.* at p.4, lines 21-32).

Referring again generally to claim 15, the second MOS transistor is provided with a source-drain path in parallel with a source-drain path of the first MOS transistor between a voltage source and reference potential. Continuing with the non-limiting example discussed above, Figure 1 of the Application clearly shows that the source-drain path of the first transistor T1 is in parallel to the source-drain path of the second transistor T2. The source-drain paths are in parallel between a voltage source +U and ground.

As claimed, the Zener diode is coupled between a gate of the first MOS transistor and a gate of the second MOS transistor. In the example of Fig. 1, a Zener diode is connected between the gates of the transistors T1 and T2. (See Fig. 1).

Independent claim 24 is directed to a MOSFET circuit that includes first and second MOS transistors and a Zener diode. The first MOS transistor has a first number of cells, and the second MOS transistor has a second, lesser number of cells. The first and second MOS transistors are integrated into the same semiconductor body. By way of non-limiting example, Fig. 1 of the Application shows a MOSFET circuit having a first MOS transistor T1 and a second

MOS transistor T2. (See Specification at p.4, line 21-23). The second transistor T2 has a lesser number of cells than the first transistor T1. (See *id.* at p.4, lines 21-32). The transistors T1 and T2 are integrated into the same semiconductor body. (See *id.* at p.6, lines 10-11).

Referring again generally to claim 24, the second MOS transistor is provided with a source-drain path in parallel with a source-drain path of the first MOS transistor between a voltage source and reference potential. Continuing with the non-limiting example discussed above, Figure 1 of the Application clearly shows that the source-drain path of the first transistor T1 is in parallel to the source-drain path of the second transistor T2. The source-drain paths are in parallel between a voltage source +U and ground.

As claimed, the Zener diode is coupled between a gate of the first MOS transistor and a gate of the second MOS transistor. In the example of Fig. 1, a Zener diode is connected between the gates of the transistors T1 and T2. (See Fig. 1).

Independent claim 30 is directed to a MOSFET circuit that includes first and second MOS transistors and a Zener diode. The first MOS transistor has a first number of cells, and the second MOS transistor has a second, lesser number of cells. The first and second MOS transistors are integrated into the same semiconductor body. By way of non-limiting example, Fig. 1 of the Application shows a MOSFET circuit having a first MOS transistor T1 and a second MOS transistor T2. (See Specification at p.4, line 21-23). The second transistor T2 has a lesser number of cells than the first transistor T1. (See *id.* at p.4, lines 21-32). The transistors T1 and T2 are integrated into the same semiconductor body. (See *id.* at p.6, lines 10-11).

Referring again generally to claim 24, the second MOS transistor is provided with a source-drain path in parallel with a source-drain path of the first MOS transistor between a

voltage source and reference potential. Continuing with the non-limiting example discussed above, Figure 1 of the Application clearly shows that the source-drain path of the first transistor T1 is in parallel to the source-drain path of the second transistor T2. The source-drain paths are in parallel between a voltage source +U and ground.

As claimed, the Zener diode is coupled between a gate of the first MOS transistor and a gate of the second MOS transistor. In the example of Fig. 1, a Zener diode is connected between the gates of the transistors T1 and T2. (See Fig. 1).

As per claim 30, the Zener diode includes a polycrystalline layer on a polycrystalline gate plane of the first and second MOS transistors and a zone provided in the polycrystalline layer and having an opposite conduction type to a conduction type of the polycrystalline layer. Fig. 3 shows a zener diode formed by the n+ zone 13 and p+ zone 14 (center), which is in the same plane as the gates 13 (right and left) of the MOS transistors. (*Id.* at p.6, line 31, p.7, line 2).

(6) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 15 and 17-34 stand rejected under 35 U.S.C. §102(b) as allegedly being obvious over U.S. Patent Publication No. US 2003/0006892A1 by Alessandria et al. (hereinafter "Alessandria") in view of U.S. Patent No. 6,851,849 to Kimura (hereinafter "Kimura"), U.S. Patent No. 4,881,024 to Hartwick (hereinafter "Hartwick"), U.S. Patent No. 6,855,981 to Kumar (hereinafter "Kumar"), U.S. Patent No. 4,937,470 to Zeiler (hereinafter "Zeiler") and U.S. Patent No. 5,438,286 to Pavlin (hereinafter "Pavlin").

Claim 35 stands rejected as allegedly being obvious over Alessandria and Pavlin in further view of U.S. Patent No. 5,917,254 to Lecce et al. (hereinafter "Lecce") in view of Rademaker et al. (hereinafter "Rademaker").

(7) ARGUMENT

I. The Rejections of Claims 15 and 17-34 Over Allesandria, Kimura, Hartwick, Kumar, Zeiler and Pavlin

The rejections of claims 15 and 17-34 are in error and should be reversed for the multiple reasons discussed below. Prior to argumentation, however, it may be helpful to explain the Final Office Action.

The Final Office Action clearly states that claims 15 and 17-34 have been rejected over Allesandria in view of Kimura, Hartwick, Kumar, Zeiler and Pavlin. (Final Office Action p.2). However, upon close review of the office Action, this does not appear to be completely accurate. A close reading of the Final Office Action reveals the following rejections:

Claim 15 appears to have been rejected as allegedly being obvious over Alessandria in view of Pavlin (See Final Office Action at p.2);

Claims 18 and 19 appear to have been rejected over Alessandria in view of Pavlin in further view of Zeiler (See Final Office Action at p.3);

Claim 20 appears to have been rejected over Alessandria in view of Pavlin in further view of Zeiler in further view of Official Notice (See Final Office Action at p.3);

Claims 21, 22, 23 and 32 appear to have been rejected over Alessandria in view of Pavlin in further view of Zeiler in further view of Kumar in further view of Official Notice (See Final Office Action at pp.3-4);

Claims 24-29 appear to have been rejected over Alessandria in view of Pavlin (See Final Office Action at p.4);

Claims 30, 33 and 34 appear to have been rejected over Alessandria in view of Pavlin (See Final Office Action at p.5);

Claim 31 appears to have been rejected over Alessandria in view of Pavlin in further view of Kumar (See Final Office Action at p.5); and

Each of the above listed "claim groups" will be discussed in one or more separate sub-headings in this section of the argument.

A. The Rejection of Claim 15 is in Error

The Examiner has rejected claim 15 as allegedly being obvious over Alessandria in view of Pavlin. (Final Office Action at p.2). As will be discussed below in detail, the Examiner has not identified a legally sufficient motivation or suggestion to combine. Moreover, the purposes of Alessandria and Pavlin are so different, one of ordinary skill in the art would not be motivated to combine those references as proposed by the Examiner.

1. Explanation of the Examiner's Rejection

It is helpful to review the Examiner's rejection of claim 15, which contains some inadvertent numbering errors. The Examiner's rejection as it stands on page 2 is set forth below:

> Regarding, claim 15, figure 10 of Alessandria shows a MOSFET circuit comprising: a first MOS transistor (23), a second MOS transistor (22) connected in parallel, a Zener diode (20) coupled between the gates of the first and second MOS transistors. Figure 2 of Pavlin shows a MOSFET circuit comprising a first transistor (TP1) and a second transistor (TP2) wherein the second transistor has less cells than the first transistor (col. 3, lines 32-50). The circuit taught by

> Pavlin has lower threshold current (IL) than the circuit having two transistors having an equal number of cells (col. 4, lines 42-62). Therefore, it would have been obvious for one of ordinary skill in the art to replace transistors (22) and (23) of Alessandria with the transistors taught by Pavlin for lowering the threshold current (total IL) thus, the power consumption of the circuit is reduced.

(Final Office Action at p.2).

A review of Figure 10 of Alessandria reveals that there is no MOS transistor labeled "(23)". This was pointed out to the Examiner in the Third Response filed by the Applicant. The Examiner did acknowledge the error in the "Response to Arguments" portion of the Final Office Action, which read:

> b. the Examiner's application of Alessandria contains inadvertent errors.
> In the previous Office Action, **only figure 10** of Alessandria was used for the rejection. In figure 10, the so-called transistor (23) was not previously labeled. For easy interpretation of the figure the Examiner labeled that transistor as (23). This label (23) is not related to element 23 of figure 5. To avoid misunderstanding, transistors (23) and (22) are relabeled as (T1) and (T2).

(Final Office Action at p.6). Thus, the Examiner has clarified that the MOS transistor of Alessandria that is referred to as MOS transistor (23) is *not* the block 23 of Fig. 5. The Examiner has also clarified that the rejection is based solely on fig. 10 of Alessandria (in view of Pavlin).

However, it may still not be clear to the Board that which the Examiner considers to be MOS transistor (T1) and MOS transistor (T2). The Examiner appears to have made notations on a copy of Figure 10 of Alessandria indicating the identity of these transistors, but neither this copy nor any notations appear on the record anywhere. (See Public PAIR image file wrapper for 10/757,974). Nevertheless, it seems clear to Applicant after studying the Final Office Action that the Examiner is referring to the MOS transistor (22) of Fig. 10 of Alessandria as (T2), and is referring to the right-hand MOS transistor of the current mirror of Fig. 10 as the transistor (T1).

It is expected that the Examiner will confirm this interpretation, and that the Appeal may move forward on this basis.

In summary, whenever the Final Office Action refers to MOS transistor (22) or MOS

transistor (T2), the Final Office Action actually is referring to the MOS transistor 22 of Fig. 10 of Alessandria. Whenever the Final Office Action refers to MOS transistor (23) or MOS transistor (T1), the Final Office Action is referring to the right-hand transistor of the unlabeled, two-transistor current mirror on the left side of Fig. 10 of Alessandria. Applicants will use the nomenclature (T1) and (T2) when referring to these transistors in the same manner.

2. No Motivation to Combine the References

The Examiner has set forth no legally sufficient motivation or suggestion to combine Alessandria and Pavlin as proposed. As will be discussed below in detail, the Examiner's reasoning on this issue contains multiple errors, each error resulting in a failure to state a prima facie case of obviousness.

In general, the Examiner admits that Alessandria fails to teach that the first MOS transistor (T1) and a second MOS transistor (T2) have a different number of cells. (Final Office Action at p.2). The Examiner states, however, that Pavlin teaches first and second MOS transistors that have a different number of cells. (*Id.*) The Examiner then alleges that Pavlin teaches that "Because of the difference of cells between two transistors, the threshold current, the total current (IL), is lower than the total current of a circuit having two transistors that have equal number of cells (col. 4, lines 41-62)." The Examiner then infers that the "Because the total current is reduced, the power consumption and the heat generated by the circuit are reduced". After this inference, the Examiner concludes that "the circuit of claim 15 fully reads on the combination of Alessandria and Pavlin and the motivation in this rejection is legally proper." (*Id.*)

a. The Examiner Mischaracterizes the Teachings of Pavlin

It is central to the Examiner's rejection that Pavlin teaches that using two transistors with a different number of cells uses less current than the amount of current used by *two transistors* with the same number cells. Thus, it would be obvious to replace two transistors with the same number of cells with two transistors having a different number of cells.

However, Pavlin does *not* teach replacing *two* transistors having the same number of cells with two transistors having a different number of cells. Pavlin teaches replacing *a single transistor* with *two* transistors, wherein the two transistors have a different number of cells. To this end, please refer to the *prior art* figure 1 of Pavlin, which shows transistors TP and TS in an open load detection circuit. Thus, the state of art according to Pavlin was a single transistor TS and a single transistor TP. Please now refer to Figs. 2 and 4 of Pavlin, which show that the *single* transistor TP has been replaced by transistors TP1 and TP2.

Moreover, please review the "Summary of the Invention" of Pavlin, which states:

> More particularly, the present invention provides a circuit for the detection of an open load for a power MOS transistor designed to operate in a switching mode. The *MOS transistor is partitioned into two transistors disposed in parallel*, the second transistor having a resistance in the conductive state higher than the resistance of the first transistor...

(Pavlin at col. 3, lines 21-27). Thus, Pavlin teaches replacing a single MOS transistor with two parallel MOS transistors.

Pavlin does not teach replacing two MOS transistors with another two MOS transistors having different cell counts. As a consequence, the Examiner's allegation that it would have been obvious to replace the two transistors T1 and T2 of Alessandria with two other transistors having different cell counts is *not* fairly suggested by Pavlin.

In addition, it is noted that the Examiner cites column 4, lines 41-62 of Pavlin as teaching the replacement of parallel transistors having the same cell count with parallel transistors having

a different cell count. This is not accurate. The passages cited by the Examiner merely describe the construction of the two MOS transistors TP1 and TP2 that replace the single MOS transistor TP. (See col. 4, lines 22-40, preceding lines 41-62).

The Examiner has therefore based the obviousness rejection on a fundamentally incorrect interpretation of Pavlin. Pavlin does not provide any motivation or suggestion to replace two transistors having an equal number of cells with two transistors having a different number of cells. Pavlin teaches replacing a single transistor with a composite transistor formed of two parallel transistors.

Referring to Alessandria, it will be appreciated that the replacement of any *single* transistor of Fig. 10 with a composite transistor as taught by Pavlin would *not arrive* at the invention. Nor does the Examiner allege as much. Instead, the Examiner alleges that it would be obvious to replace the transistors T1 and T2 with a *composite transistor TP1, TP2* taught by Pavlin. As discussed above, the prior art simply contains no motivation or suggestion to make such a replacement.

b. Alessandria and Pavlin have Different Purposes

Even if Pavlin were assumed to teach the replacement of two parallel transistors with two other parallel transistors having different cell counts, which it does not, Pavlin does not teach that such a replacement is useful in a voltage stabilization circuit such as that of Alessandria.

In particular, the circuits of Alessandria and Pavlin serve vastly different purposes, and the prior art does not fairly suggest that the advantages taught by Pavlin of using different numbers of cells in separate transistors would serve any purpose in the circuit of Alessandria.

To this end, Pavlin teaches an *open load detection* circuit that has a very low detection threshold. The low detection threshold is desirable "in order to differentiate the case when the charging current is low because the load has a high value from the case when the current is low, or zero because the load is open" (Pavlin at col. 1, lines 52-58). To achieve a low detection threshold, Pavlin introduces a composite transistor TP made up of two MOS transistors TP1 and TP2 having separately driven gates, and vastly different numbers of cells. (*Id.* at col. 4, lines 23-62).

Alessandria is not an open load detection circuit. Alessandria does not have a need for a low detection threshold similar to Pavlin. None of the prior art teaches that a voltage stabilization circuit such as that of Alessandria has or requires a low detection threshold. The teachings of Pavlin simply have no application to Alessandria.

The Examiner infers, however, that "because the total current is reduced [by replacing two transistors with equal cells with two transistors with different numbers of cells], the power consumption and the heat generated by the circuit are reduced". There is no teaching or suggestion that such saving is possible in the circuit of Alessandria. More specifically, in Pavlin, the transistors TP1 and TP2 have source/drain paths connected to a load. (See Pavlin Fig. 2). As a result, the source-drain current level is an important consideration. In Alessandria, the transistors T1 and T2 are part of a *voltage* protection circuit, and have no load connected in their source/drain paths. The current issues present in Pavlin are not present in Alessandria.

Because of the vast difference in purposes and uses of the transistors in Pavlin and Alessandri, there is no legally sufficient motivation or suggestion to replace the parallel transistors of Alessandri with the parallel transistors of Pavlin as proposed by the Examiner.

c. Conclusion as to Claim 15

For the foregoing reasons, it is respectfully submitted that there is no legally sufficient motivation or suggestion to combine Alessandria as proposed by the Examiner in the Final Office Action. The Examiner has therefore failed to set forth a prima facie case of obviousness with respect to claim 15. As a consequence, the obviousness rejection of claim 15 should be reversed.

B. The Rejection of Claims 18 and 19 are in Error

Claims 18 and 19 stand rejected over Alessandria, Pavlin and Zeiler. Claims 18 and 19 depend from and incorporate all of the limitations of claim 15. As an initial matter, the rejection of claims 18 and 19 rely on the combination of Alessandria and Pavlin as cited against claim 15. As discussed above, there is no motivation or suggestion to combine Alessandria and Pavlin as proposed. As a consequence, the obviousness rejections of claims 18 and 19 should be reversed for at least the same reasons as those set forth above in connection with claim 15.

In addition, the rejections of claims 18 and 19 should be reversed for *additional independent reasons.* Claims 18 and 19 both include a limitation directed to "a first resistor connected in parallel to the Zener diode".

As clearly shown in Fig. 10 of Alessandria, there is no resistor connected in parallel to the Zener diode 20. The Examiner further admits that the proposed combination of Alessandria and Pavlin fails to include the resistor in parallel to the Zener diode. (Final Office Action at p.3). Nevertheless, the Examiner alleges that it would be obvious to replace the single diode of Alessandria with the diode and resistor taught by Zeiler.

Applicants disagree. Zeiler teaches the use of a Zener diode and parallel resistor in a

completely different context than that of the Zener diode of Pavlin. As will be discussed below in detail, no one of ordinary skill in the art would be motivated by the use of a parallel diode and resistor in the context of Zeiler to modify the circuit of Alessandria.

1. The Zener Use in Alessandria is Completely Unrelated to the Zener Use in Zeiler

Allesandria shows a Zener diode 20 that provides an output voltage regulation function. In particular, the Zener diode 20 is used to prevent turning on of the transistor 22 (i.e. T2) until the output voltage V_o overcomes the Zener threshold. Accordingly, the Zener diode 20 is coupled reverse biased from the V_o to the gate of the transistor 22 ("T2"), and is further coupled to ground via a resistor. (See Fig. 10 of Alessandria).

By contrast, the Zener diode 44 of Zeiler is forward biased into the gate of a transistor. In addition, the Zener diode 44 of Zeiler is not coupled to ground, and does not require the Zener threshold to be overcome to turn on the corresponding MOS transistor. The Zener diode 44 is used for a completely different purpose in Zeiler than the Zener diode of Alessandria. No one of ordinary skill in the art would find a motivation to add a resistor in parallel to the Zener diode of Alessandria based on the teachings of Zeiler. Not only are the uses completely different, but the Zener diodes are not even oriented the same way with respect to the gates of their corresponding transistors.

For at least this reason, the rejection of claims 18 and 19 should be reversed.

2. The Examiner's Reasoning for the Combination

The Examiner set forth the following argument with respect to the modification of Alessandria and Pavlin with the parallel resistor of Zeiler:

> The circuit of ... Alessandria has a limitation that the voltage applied to the gate of transistor (T2) only happens when the input voltage (Vin) is high enough to reverse biased Zener (20). Figure 1 of Zeiler shows a Zener diode (44) having a resistor (46) coupled in parallel with it for continuously controlling the second MOS transistor (T2) and for limiting the voltage applied to the gate of the second MOS transistor. Therefore, it would have been obvious for one of ordinary skill in the art to replace the single diode (20) of Alessandria with the diode and the resistor taught by Zeiler for continuously controlling the second MOS transistor (T2) and for limiting the voltage applied to the gate of the second transistor.

(Final Office Action at p.3). Applicants disagree.

The Examiner states that the "circuit of Alessandria *has a limitation* that the voltage applied to the gate of the transistor (T2) only happens when the input voltage (Vin) is high enough to reverse [bias] Zener (20)". This is an arbitrary statement without any support whatsoever in the prior art of record. Specifically, the Examiner does not cite where the prior art teaches that this is a "limitation" of Alessandria. In fact, it is unfathomable how this could be considered a limitation of Alessandria. Alessandria specifically teaches that the voltage is applied to the gate of the transistor 22 when the input voltage is high enough to reverse bias the Zener 20. That is what it is intended to do. Nowhere does the prior art suggest that the Zener diode 20 in the circuit of Figure 10 of Alessandria, *or any circuit remotely similar thereto,* represents a limitation to the operation of the circuit.

While the lack of a resistor may or may not be a limitation of the circuit of Zeiler, that circuit so vastly differs in operation and purpose, such that no one ordinary skill in the art would infer such a limitation to the circuit of Alessandria.

The Examiner further states that the presence of a parallel resistor in the Alessandria circuit would allow for "continuous control" of the second MOS transistor. Again, the prior art does not teach that 1) adding such a parallel resistor would provide "continuous control" in the circuit of Alessandria, or 2) that such "continuous control" would be of the slightest advantage in Alessandria. Again, the basis for the combination appears to be arbitrary and without any support in the record.

3. Conclusion as to Claims 18 and 19

For the foregoing reasons, the rejection of claims 18 and 19 should be reversed for reasons additional to those set forth above in connection with claim 15. In particular, there is not the *slightest* motivation or suggestion to modify Alessandria and Pavlin with the parallel resistor of Zeiler, much less a legally sufficient motivation or suggestion.

C. The Rejection of Claim 20 is in Error

Claim 20 stands rejected over Alessandria, Pavlin and Zeiler. Claim 20 depends from and incorporates all of the limitations of claim 19. The rejection of claim 20 relies on the combination of Alessandria, Pavlin and Zeiler as cited against claim 19. As discussed above, there is no motivation or suggestion to combine any of Alessandria, Pavlin or Zeiler as proposed. As a consequence, the obviousness rejection of claims 20 should be reversed for at least the same reasons as those set forth above in connection with claim 19.

D. The Rejection of Claims 21, 22 and 23 are in Error

Claims 21, 22 and 23 stand rejected over Alessandria, Pavlin, Zeiler, Kumar and Official Notice. Claims 21, 22 and 23 depend from and incorporate all of the limitations of claim 19 (via claim 20). As an initial matter, the rejection of claims 21, 22 and 23 relies on the combination of Alessandria, Pavlin and Zeiler as cited against claim 19. As discussed above, there is no motivation or suggestion to combine any of Alessandria, Pavlin or Zeiler as proposed. As a consequence, the obviousness rejections of claims 21, 22 and 23 should be reversed for at least the same reasons as those set forth above in connection with claim 19.

In addition, the rejections of claims 21, 22 and 23 should be reversed for *additional independent reasons.* Claims 21, 22 and 23 all include the following limitation:

> ...wherein the Zener diode and the first resistor are formed by a highly doped polycrystalline layer of a first conduction type and a polycrystalline layer of a second conduction type that is in contact with the highly doped polycrystalline layer.

The Examiner has not alleged a prima facie case of obviousness with respect to claims 21, 22 and 23. The Examiner appears to admit that Alessandria, Pavlin and Zeiler fail to teach the structural limitations of the Zener diode and first resistor in claims 21, 22 and 23. To address these limitations, the Examiner states that, "the technique of fabrication of the zener diode and the resistor are well known in the art and is fully shown by Kumar ..." (Final Office Action at p.3).

However, the Examiner never alleges that it would have been obvious to modify Alessandria, Pavlin or Zeiler to include Zener diodes or resistors fabricated in this manner. The Examiner certainly never alleges a motivation or suggestion to perform such a modification.

An obviousness rejection cannot be supported by a mere citation to multiple references that, if combined in some manner, arrive at the invention. The Examiner must identify a motivation or suggestion to combine elements of the references. In the rejection of claims 21, 22 and 23, the Examiner merely alleges that Zener diodes and resistors of the having the limitations of claim 21 are known. The Examiner never alleges why such Zener diodes or resistors would be used in the circuit formed by the combination of Alessandria, Pavlin or Zeiler.

As a consequence, the Examiner has failed to allege a prima facie case of obviousness. The rejection of claims 21, 22 and 23 should therefore be reversed on at least this independent ground.

E. The Rejection of Claims 24-29 are in Error

Claims 24-29 stand rejected over Alessandria and Pavlin. Independent claim 24 includes limitations similar to those of claim 15. The rejection of claim 24 relies on the combination of Alessandria and Pavlin as cited against claim 15. As discussed above, there is no motivation or suggestion to combine Alessandria and Pavlin as proposed. As a consequence, the obviousness rejection of claim 24 should be reversed for at least the same reasons as those set forth above in connection with claim 15. Moreover, claims 25-29 depend from claim 24. As a result, the obviousness rejection of claims 25-29 should be reversed for at least the same reasons.

F. The Rejection of Claims 30, 31, 33 and 34 are in Error

Claims 30, 31, 33 and 34 stand rejected apparently over Alessandria, Pavlin and, at least with respect to claim 31, Kumar. (See Final Office Action at p.5). Independent claim 30 includes limitations similar to those of claim 15. The rejection of claim 30 relies on the combination of Alessandria and Pavlin cited against claim 15. As discussed above, there is no motivation or suggestion to combine Alessandria and Pavlin as proposed. As a consequence, the obviousness rejection of claim 30 should be reversed for at least the same reasons as those set forth above in connection with claim 15. Moreover, claims 31, 33 and 34 depend from claim 30. As a result, the obviousness rejection of claims 31, 33 and 34 should be reversed for at least the same reasons.

In addition, the rejections of claims 30, 31, 33 and 34 should be reversed for *additional independent reasons.* Claims 30, 31, 33 and 34 all include the following limitation:

> ...said Zener diode comprising a polycrystalline layer on a polycrystalline gate plane of th first and second MOS transistors and a zone provided in the polycrystalline layer and having the opposite conduction type to a conduction type of the polycrystalline layer.

The Examiner has made no allegation that this limitation is taught by the prior art in connection

with the rejection of claims 30, 31, 33 and 34. Accordingly, the Examiner has not alleged a combination that arrives at the invention of any of claims 30, 31, 33 or 34. No combination of Alessandria and Pavlin arrives at the invention of claim 30.

It is possible that the Examiner intended to reject claim 30 over Alessandria, Pavlin and Kumar. (Kumar is mentioned in the rejection of claim 31, but not for the purposes of satisfying the limitations of claim 30). Even if this were true, the Examiner has identified no motivation or suggestion to combine the teachings of Kumar with either Pavlin or Alessandria, as discussed above in connection with claims 21, 22 and 23.

Accordingly, the Examiner has not alleged a prima facie case of obviousness with respect to claims 30, 31, 33 and 34. The rejection of claims 30, 31, 33 and 34 should be reversed on at least this independent ground.

G. Claim 32

Claim 32 stands rejected over Alessandria, Pavlin, Zeiler, Kumar and Official Notice. (Final Office Action at p.3). As discussed above, the Examiner has not set forth a legally sufficient motivation or suggestion to combine Alessandria and Pavlin. As also discussed above, the Examiner has not alleged *any* motivation or suggestion to combine Kumar with any of Alessandria, Pavlin or Zeiler.

For at least these reasons, the obviousness rejection of claim 32 should be reversed.

II. The Rejection of Claim 35 is in Error

Claim 35 stands rejected apparently over Alessandria, Pavlin, Lecce and Rademaker. (See Final Office Action at p.5). Claim 35 depends from and includes all of the limitations of

claim 15. As discussed above, there is no motivation or suggestion to combine Alessandria and Pavlin as proposed to arrive at the invention of claim 15. As a consequence, the obviousness rejection of claim 35 should be reversed for at least the same reasons as those set forth above in connection with claim 15.

In addition, the rejection of claim 35 should be reversed for *additional independent reasons.* Claim 35 all include the following limitation:

> ...wherein the Zener diode is forward biased from the control input [of the circuit] to the gate of the second MOS transistor.

The Examiner has alleged that reversing the biasing of the Zener diode of Alessandria would have been a design expedient, because it would have raised the threshold voltage at the gate of the MOS transistor T2 of Alessandria. (Final Office Action at p.6).

The prior art does not fairly suggest that Alessandria would benefit from reversing the bias of the Zener diode 20 in Figure 10. To the contrary, it would defeat the entire purpose of the circuit. (See Alessandria at Figs. 2, 5, 10 and at paragraph [0019]). The reverse-bias Zener in Alessandria acts as a voltage regulator. A forward-biased Zener in Allesandria would not.

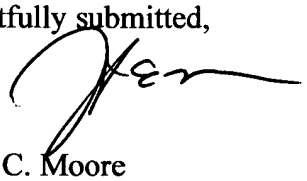
For at least this reason, it is submitted that the Examiner has failed to set forth a legally sufficient motivation or suggestion to combine Alessandria and Pavlin with the combined teachings of Lecce and Rademaker.

Accordingly, the Examiner has not alleged a prima facie case of obviousness with respect to claim 35. The rejection of claim 35 should be reversed on at least this independent ground.

(8) CONCLUSION

For all of the foregoing reasons, claims 15 and 18-35 are not unpatentable. As a consequence, the Board of Appeals is respectfully requested to reverse the rejection of these claims.

Respectfully submitted,



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CLAIM APPENDIX

15. A MOSFET circuit comprising:

- a first MOS transistor having a first number of cells,
- a second MOS transistor having a second number of cells, the second number being less than the first number and the second MOS transistor being provided with a source-drain path in parallel with a source-drain path of the first MOS transistor between a voltage source and reference potential, and
- a Zener diode coupled between a gate of the first MOS transistor and a gate of the second MOS transistor.

18. The MOSFET circuit as claimed in claim 19, further comprising a second resistor connected in series with a parallel circuit formed by the Zener diode and the first resistor.

19. The MOSFET circuit as claimed in claim 15, further comprising a first resistor connected in parallel with the Zener diode.

20. The MOSFET circuit as claimed in claim 19, wherein
the Zener diode and the first resistor are integrated with one another.

21. The MOSFET circuit as claimed in claim 20, wherein the Zener diode and the first resistor are formed by a highly doped polycrystalline layer of a first conduction type and a polycrystalline layer of a second conduction type that is in contact with the highly doped polycrystalline layer.

22. The MOSFET circuit as claimed in claim 21, wherein the polycrystalline layer of the second conduction type is located on a polysilicon gate plane of the MOSFET circuit.

23. The MOSFET circuit as claimed in claim 21, wherein

a doping concentration of the highly doped layer is less than 10^{19} charge carriers cm^{-3}.

24. A MOSFET circuit comprising:

- a first MOS transistor having a first number of cells, the first MOS transistor integrated into a semiconductor body;
- a second MOS transistor having a second number of cells, the second MOS transistor integrated into the semiconductor body, the second number being less than the first number and the second MOS transistor being provided with a source-drain path in parallel with a source-drain path of the first MOS transistor between a voltage source and reference potential, and
- a Zener diode coupled between a gate of the first MOS transistor and a gate of the second MOS transistor.

25. The MOSFET circuit as claimed in claim 24, wherein the first number of cells is at least twice the second number of cells.

26. The MOSFET circuit as claimed in claim 25, wherein the first number of cells is at least ten times the second number of cells.

27. The MOSFET circuit as claimed in claim 25, wherein the first number of cells is approximately 1000.

28. The MOSFET circuit as claimed in claim 24, wherein the first MOS transistor and the second MOS transistor comprise CoolMOS transistors.

29. The MOSFET circuit as claimed in claim 24, wherein the semiconductor body is of a second conduction type and charge compensation regions of a first conduction type are incorporated into the semiconductor body.

30. An integrated MOSFET circuit comprising:

- a first MOS transistor having a first number of cells, said transistor being integrated in a semiconductor body,
- a second MOS transistor having a second number of cells, said transistor being integrated in the semiconductor body, the second number being less than the first number and the second MOS transistor being provided with a source-drain path in parallel with a source-drain path of the first MOS transistor between a voltage source and a reference potential, and
- a Zener diode connected between a gate of the first MOS transistor and a gate of the second MOS transistor, said Zener diode comprising a polycrystalline layer on a polycrystalline gate plane of the first and second MOS transistors and a zone provided in the polycrystalline layer and having an opposite conduction type to a conduction type of the polycrystalline layer.

31. The integrated MOSFET circuit as claimed in claim 30, further comprising a resistor connected in parallel with the Zener diode, the resistor formed by the pn junction between the polycrystalline layer and the zone.

32. The integrated MOSFET circuit as claimed in claim 31, wherein the doping concentration of the zone is less than 10^{19} charge carriers cm^{-3}.

33. The MOSFET circuit as claimed in claim 30, wherein the first number of cells is at least twice the second number of cells.

34. The MOSFET circuit as claimed in claim 30, wherein the first number of cells is at least ten times the second number of cells.

35. The MOSFET circuit as claimed in claim 15, wherein the Zener diode is further coupled between the gate of the second MOS transistor and a control input of the MOSFET circuit, and wherein the Zener diode is forward biased from the control input to the gate of the second MOS transistor.

EVIDENCE APPENDIX

NONE

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RELATED PROCEEDINGS APPENDIX

NONE

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